Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY

Summer Examination-2017

Subject Name: Computer Organization & Architecture

Subject Code: 4TE04COA1 Branch: B.Tech (CE)

Semester: 4 Date : 08/05/2017 Time : 02:00 To 05:00 Marks : 70

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

Q-1 **Define the following terms:** **(14)**

a) Instruction code
b) Micro Operation.
c) LDA.
d) BUN.
e) ISZ.
f) STA.
g) Subroutine
h) Register Transfer Language.
i) Pipeline
j) Effective Address
k) Firmware
l) SKI.
m) Bus.
n) Interrupt.

Attempt any four questions from Q-2 to Q-8

Q-2 **Attempt all questions** **(14)**

(a) Explain Common Bus System with Architecture. **(7)**
(b) Explain Binary Adder – Subtractor. **(7)**

Q-3 **Attempt all questions** **(14)**

(a) Explain Direct Address and Indirect Address. **(7)**
(b) What is Instruction Cycle? Explain Instruction Cycle with Flow Chart. **(7)**

Q-4 **Attempt all questions** **(14)**

	(a)	Explain Shift Micro operation with different types.	**(7)**
	(b)	What is RPN? Give one example for evaluation of arithmetic expressions.	**(7)**
Q-5		**Attempt all questions**	**(14)**
	(a)	List out name of Addressing Mode. Explain any three Addressing modes.	**(7)**
	(b)	Explain different types of interrupts in basic computer.	**(7)**
Q-6		**Attempt all questions**	**(14)**
	(a)	Explain General Register Organization with Architecture.	**(7)**
	(b)	Differentiate RISC and CISC.	**(7)**
Q-7		**Attempt all questions**	**(14)**
	(a)	Explain Stack Organization in the form of Memory Stack.	**(7)**
	(b)	Explain Bus and Memory Transfer with Architecture.	**(7)**
Q-8		**Attempt all questions**	**(14)**
	(a)	Explain Parallel Processing with multi-functional units.	**(7)**
	(b)	Explain Pipeline Processing with Example.	**(7)**